IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, L.L.C., Plaintiffs, v. SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C., Defendants.	C.A. No. 07-449 (JJF) **REDACTED PUBLIC VERSION**
SAMSUNG ELECTRONICS CO., LTD., SAMSUNG ELECTRONICS AMERICA, INC., SAMSUNG TELECOMMUNICATIONS AMERICA GENERAL, L.L.C., SAMSUNG SEMICONDUCTOR, INC., and SAMSUNG AUSTIN SEMICONDUCTOR L.L.C., Plaintiffs, v. ON SEMICONDUCTOR CORP. and SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC, Defendants.	C.A. No. 06-720 (JJF)

DECLARATION OF MARTIN G. WALKER, Ph.D. IN SUPPORT OF THE REPLY BRIEF OF ON SEMICONDUCTOR CORP. AND SEMICONDUCTOR COMPONENTS INDUSTRIES, LLC IN SUPPORT OF THEIR MOTION TO COMPEL DISCOVERY

I, Martin G. Walker, Ph.D., declare as follows:

1. I have been retained as an expert consultant by the law firm of Jones Day, counsel of record for ON Semiconductor in the above-captioned matters. This declaration is based on

Redacted Filing Date: March 4, 2008

my personal knowledge and experience as well as my investigation in this matter and reflects my expert opinions on certain issues.

2. My CV (Exhibit A) contains an overview of my thirty years of experience in the field of Electronic Design Automation ("EDA") software systems. I received a BSEE from the Massachusetts Institute of Technology in 1973, and MSEE from Stanford University in 1976, and a PhD. in electrical engineering from Stanford University in 1979. My work experience includes direct work with EDA software, both as a developer and as a designer.

3. From 1983 to 1989, I was the founder and Chief Technical Officer at Analog Design Tools, Inc. In my work at Analog, I was a founder and founding CEO. I was primarily responsible for writing the original business plan and raising the venture capital necessary to launch the company and recruiting the staff. Later, I was responsible for all technical aspects of product definition and development. My efforts were instrumental in growing Analog from a start-up company to a leader in the field of analog design automation.

4. From 1990 to 1994, I was a founder and Executive Vice President of Symmetry Design System ("Symmetry"), which specialized in product design and consulting for the electronic design marketplace. In this role, I was instrumental in development of Symmetry's products.

5. In 1995, I founded a company called Frequency Technology (now Sequence Design) ("Sequence") that develops EDA software for the design of advance system-on-a-chip integrated circuits. Sequence's products have become the *de facto* industry standard for parasitic extraction, circuit optimization, and RTL power analysis. As Chief Executive Office, director, and Chief Scientist at Sequence, I was involved in overseeing the development of the company's products and technologies. I also took an active role in recruiting the technical and business staff.

6. I am named as an inventor in three patents in the field of electronic design automation.

7. I am familiar with the processes for designing and manufacturing semiconductor products. I have used various EDA design tools, including those from Synopsys, Cadence, and Mentor Graphics, to both design and analyze circuits. These tools are very expensive, costing over $100,000, and time consuming to acquire and set up. Because modern semiconductor products are very complex, it is virtually impossible to design and analyze them without EDA tools.

8. Attached as Exhibit B is an excerpt from a text ("Application-Specific Integrated Circuits" by Michael John Sebastian Smith) that describes the process of designing semiconductor products. As can be seen in Exhibit B, pg. 17, there are two broad steps in creating the design of a device: "logical design" and "physical design." The result of the logical design process is generally a netlist. A schematic is a graphical representation of a netlist. Netlists are usually maintained by EDA tools in a hierarchical database. The best way to evaluate circuits is to use EDA tools which access the native databases of the circuits at issue. The output of the physical design process is normally a GDS2 file. The physical design is also maintained by the EDA tools in a hierarchical database.

9. EDA design tools can be used to design and analyze circuitry through the use of netlists and schematics. In particular, EDA tools analyze designs using the netlist; people sometimes prefer to use schematics, usually integrated into the EDA tools, so that the tools can be used to navigate the schematics. Since electronic devices are complex, containing millions of transistors, it is very difficult, burdensome, and time consuming to determine functionality of an electronic device by reviewing schematics separate from the EDA tools. For example, through

the use of these schematic design tools, one would be able to navigate up or down in the hierarchy of a circuit design. The high-level view of a design can be useful to identify where certain general functionality is performed. Once an area of interest is identified, the schematic design tools then allow for traversing down the hierarchy to see the details of a particular functional block, for example, allowing for a circuit to be viewed at a lower logic level or at an even lower transistor level. This is illustrated in Exhibit B by the flow from box 2 ("logic synthesis") to box 4 ("prelayout simulation").

10. Schematic design tools also allow for signals to be traced throughout a circuit, including between circuit blocks, and further allow for the viewing of the attributes of a particular semiconductor device at any point of the design. More importantly, EDA design tools allow for the simulation of the circuit being designed or analyzed. This is crucial because of the complexity of modern circuits. Whereas a small block of circuitry may be analyzed manually (i.e., without EDA tools), its operation in the larger context of the entire circuit is much more complex and virtually impossible without EDA tools.

11. It is my understanding that Samsung originally produced images of certain schematics in TIFF format. It is my further understanding that Samsung subsequently produced the same information in PDF and PS files. I am familiar with these types of files. PDF (Portable Document Format) and PS (PostScript) files are proprietary file formats from Adobe Systems and are basically the equivalent of paper print-outs of the schematics. These image files are not the manner in which analysis and design information is kept by companies such as Samsung. Image files such as PDF and PS files do not provide the design and analysis functionality of EDA tools as described in paragraphs 9 and 10, above. For example, PDF and PS files are not navigable for traversing the hierarchy of a circuit.

12. I am familiar with modern memory products such as those accused of infringing in the present case. These products contain many millions of transistors. But I understand that Samsung has only produced from 71-184 pages of schematics for each particular accused product. For example, I specifically understand that Samsung produced 184 pages of images of schematics to represent one of its 512 megabyte memory products, i.e., a memory product with 512 million bits of information. Based on my experience in the semiconductor industry, it is inconceivable that the complex memory circuits with its millions of transistors can be completely represented in 184 pages of images. A schematic database, however, can fully represent the accused memory products.

13. As mentioned above, EDA tools are also used to design the physical placement of circuitry within a semiconductor die as well as to design the physical connectivity of such circuitry. Proper physical placement is crucial to the correct operation of a final product. Because of the complexity of modern circuit, this design step cannot be performed without computerized EDA tools. Physical design information is typically represented as GDS2 (or GDSII) data. Only after the physical design is complete and known to operate as desired is GDS2 information sent to a foundry for production. GDS2 data is used by a foundry to create the actual masks used to manufacture parts. Such mask data is often maintained in a file format called "MEBES." MEBES files are distinct from GDS2 files, and contain different data including many structures necessary to realize the desired design that are not in the GDS2 data.

14. The physical design of a circuit must correspond to the schematic design (or idealized design). In this way, schematic and GDS2 data have corresponding but not identical information. For example, where a schematic may identify the interconnectivity of a first and second transistor, there must be corresponding first and second transistors in the GDS2 data. But

where the interconnectivity in a schematic is represented by an idealized wire connection, the GDS2 data includes information about the real-world characteristics of the wire. For example, the GDS2 data would have information about the length and width of the interconnecting metal lines. This real-world information can then be used to more properly characterize and simulate a circuit design. This process is illustrated in Exhibit B by the flow from box 8 ("circuit extraction") to box 9 ("postlayout simulation"). Real-world physical layout information, such as contained in GDS2 databases, is very important in analyzing the timing characteristics of a circuit as well as providing a link between what is theoretically designed using schematic design tools and what is actually manufactured and sold.

15. I am familiar with the manner in which design information is kept in the normal course of business of companies such as Samsung. Design information is typically kept in schematic and layout databases. These databases are the foundation of the design process and are the best tools for designing and analyzing circuitry.

I DECLARE UNDER PENALTY OF PERJURY that the foregoing is true and correct.

Executed on February 28, 2008, in Palo Alto, California.

Martin Walker

CERTIFICATE OF SERVICE

I, the undersigned, hereby certify that on March 4, 2008, I electronically filed the foregoing with the Clerk of the Court using CM/ECF, which will send notification of such filing(s) to the following:

Josy W. Ingersoll
John W. Shaw
Andrew A. Lundgren

I also certify that copies were caused to be served on March 4, 2008 upon the following in the manner indicated:

BY HAND AND EMAIL

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EXHIBIT A

Martin G. Walker, Ph.D.
Curriculum Vitae

Professional Summary

Dr. Walker has over 25 years experience in electronic design automation (EDA) software systems, circuit simulation and circuit design. He is a recognized expert in the field of EDA systems, simulation, and modeling. He also has considerable experience in web applications development and management of high availability web-based systems.

Employment History

From: 2001 **Brass Rat Group, Inc.**
To: Current Woodside, CA
Position: *CEO*

Brass Rat Group is a successful Silicon Valley based consulting organization specializing in litigation consulting and business consulting in the electronic design automation (EDA) field. Dr. Walker has also been engaged in source-code copying litigation, offering opinions in patent, copyright, and trade secret aspects.

From: 2000 **Knowledge Networks**
To: 2001 Menlo Park, CA
Position: *Chief Technology Officer*

Knowledge Networks is a pre-IPO market research company that is leveraging internet technology to revolutionize the market research industry. KN recruited a panel of over 50,000 consumers to be interviewed on a variety of topics weekly. Dr. Walker managed KN's engineering group, which designed and created automated systems to create surveys, conduct interviews, process data, and manage the panel. He also managed the IT group which was responsible for high-availability web-based systems for fielding the interviews as well as the internal systems required to analyze the data and produce real-time reports.

From: 1995 **Sequence Design (Formerly Frequency Technology)**
To: 2000
Position: *Founder, Founding CEO, Director & CTO*

Sequence Design, formerly Frequency Technology, is the leader in the EDA segment called Design Closure. Sequence's products and services, consisting of pre- and post-layout optimization based on accurate layout extraction, enable designers to bring higher performance, lower-power integrated circuits quickly to tape out. Dr. Walker:

- Developed business plan and raised over $9MM in financing;
- Hired staff and led development, including defining technical product definition;
- Personally developed many of the basic algorithms, which resulted in

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five issued patents;
- Led initial marketing efforts;
- Wrote numerous technical articles advancing the company's technical position;
- Served as chief technical spokesman for the company.

From: 1990 **Symmetry Design Systems**
To: 1995 Los Altos, CA
Position: *Founder, Director & Executive Vice President*

Symmetry, a self-funding enterprise, was a service and product business specializing in the analog simulation EDA market. Products included simulation-model libraries, modeling tools, and special-purpose analog simulators. Dr Walker was responsible for a joint venture in Beijing China, where new products were developed. Symmetry was acquired by Analogy, Inc.

- Initiated Japanese and European marketing activities.
- Developed conceptual framework and user-interface model for the Sun OpenLook-based product.
- Served as technical spokesman in customer and industry forums.
- Conducted sales training in the US, Asia, and Europe.

From: 1983 **Analog Design Tools**
To: 1990 Sunnyvale, CA
Position: *Founder, Director, Founding CEO & Chief Scientist*

ADT's first product, the Analog WorkBench, pioneered the market for Analog CAE workstations, including such fundamental concepts as multiple window CAE systems, and simulated test instruments as a paradigm for CAE user interface. ADT, which had grown to $16MM in annual sales and 150 employees, was acquired by Cadence.

- Formulated original business plan and presented concept to venture investors. Raised initial venture financing. Led fund-raising activities through the series C round.
- Served as President during formative stage. Director and Chief Scientist (CTO) from the founding through acquisition. Set the product direction. Drove the technology development.
- Formulated ADT's initial marketing strategy. The international distribution strategy focused primarily on Japan.
- Developed the Japanese market for ADT's products. Responsible for establishing and maintaining our distributor relationship, negotiating contracts, supporting customers, and building sales that amounted to 20% of the installed base.

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From:	1980	**COMSAT**
To:	1983	Palo Alto, CA
	Position:	*Director, Microwave Systems*
		Managed a Navy sponsored program to develop high productivity techniques for manufacturing of microwave components. Developed a microwave circuit-synthesis product.

From:	1973	**Watkins-Johnson**
To:	1980	Palo Alto, CA
	Position:	*Member of the Technical Staff*
		Developed GaAsMESFET-based microwave amplifiers, components, and tuners. Designed and produced the world's first GaAsMESFET amplifiers to be delivered in production quantities.

Consulting History (within last 5 years)

From:	2005	**Sequence Design**
To:	Current	Santa Clara
	Duties:	EDA software analysis

From:	2005	**Sabio Labs**
To:	2005	Palo Alto, CA
	Duties:	Create business plan, operating plan, and marketing plan for EDA startup focused on analog circuit optimization and synthesis

Litigation Support Experience

Dr. Walker has testified in a jury trial involving technology software issues and in an arbitration. Dr. Walker also has significant experience in giving deposition testimony and in crafting declarations and expert reports. Dr. Walker regularly works with attorneys to help articulate and manage the many technology issues that arise in complex litigation.

Date:	2000-02	**Thelen Reid (for Plaintiff)**
	Case	Sequence Design vs various defendants
	Project:	Patent infringement relating to EDA software (I am an inventor of the patents at issue). Provided support for claim construction and infringement analyses.
	Status:	Settled

Date:	2001-03	**Dechert, LLP (for Plaintiff)**
	Case	Silvaco v Antonau (CSI)
	Project:	Misappropriation of trade secrets, including copied source code. Analysis of source code. Worked directly with attorneys and plaintiff; provided numerous declarations that supported this description. Testified at

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deposition regarding source code copying, other trade secret misappropriation, and business practices.

Status: Judgment entered against CSI, other claims settled on terms favorable to plaintiff

Date: 2001-02 **FTI Teklicon (for IRS)**
Case IRS vs taxpayer
Project: Analysis of valuation for tax purposes of EDA software and associated royalty streams.
Status: Completed

Date: 2001-02 **Dechert LLP (for Plaintiff)**
Case Synopsys vs Nassda (patent infringement – '053)
Project: Declaration, expert report, and deposition in support of claim construction. Declaration in opposition to Summary Judgment motion for non-infringement that was denied by the Court. Infringement analysis and expert report. Opposition to invalidity claims.
Status: Settled

Date: 2001-04 **Dechert, LLP (for Plaintiff)**
Case Synopsys vs Nassda (State Action)
Project: Identification of misappropriated trade secrets. Analysis of source code creation rates. Analysis of electronic evidence tampering. Assist with discovery issues. Manage electronic discovery of more than 300Gbytes of documents. Analysis and declarations regarding disk wiping and other evidence tampering by defendants.
Status: Settled

Date: 2001 **Law offices of Al Reynaldo (for cross-defendant Aprés)**
Case Aprés vs Ho
Project: Misappropriation of EDA-related trade secrets. Testified at trial.
Status: Settled

Date: 2003-04 **Dechert LLP (for Plaintiff)**
Case Synopsys vs Nassda (patent infringement – '998)
Project: Claim construction analysis and declaration. There were 11 disputed terms. The Court adopted Dr. Walker's construction on all 11 terms, rejecting all of the defendants arguments.
Status: Settled

Date: 2003-04 **Dechert LLP (for Respondent)**
Case CSI vs Silvaco
Project: Arbitration resulting from alleged violation of the terms of the settlement agreement. Testified for two days regarding the CSI's licensing, support and maintenance of certain Silvaco trade secrets.

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	Status:	Arbitration completed
Date:	2003-04	**Dechert LLP (for Plaintiff)**
	Case	HCL vs eKomas
	Project:	Analysis and identification of directly copied source code. The product at issue is a web-based application for loan management.
	Status:	Settled
Date:	2004	**McDermott (for Defendant)**
	Case	Tera Systems vs InTime Software
	Project:	Patent infringement related to EDA software. Researched invalidity and supported claim construction.
	Status:	Settled
Date:	2004-05	**Dechert LLP (for Plaintiff)**
	Case	Silvaco vs CSI – OSC re Contemp
	Project:	Analysis and declaration regarding the Defendants' continued use of Silvaco trade secrets.
	Status:	Completed
Date:	2004-05	**Dechert LLP (for Defendant)**
	Case	Siliconix vs AATI
	Project:	Patent infringement regarding method for manufacturing a semiconductor device. Support for claim construction and invalidity analysis. Researched prior art.
	Status:	Settled
Date:	2005	**Kirkland & Ellis LLP (for Defendant)**
	Case	Berry vs Fleming, et al.
	Project:	Source code copyright and misappropriation of trade secrets. Reviewed source code at issue. Expert report and declarations in support of summary judgment.
	Status:	Ongoing
Date:	2005	**Dechert LLP (for Plaintiff)**
	Case	Synopsys vs Magma
	Project:	Patent infringement regarding method EDA software. Support for claim construction and invalidity analysis. Supported source code analysis.
	Status:	Ongoing
Date:	2005	**Browne & Woods LLP (for Defendant)**
	Case	Keywords vs ISE
	Project:	Investigated allegations of source code copying and copyright infringement. Declaration ISO of opposition to preliminary injunction.
	Status:	Settled

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Date:	2005	**Jones, Day (for Plaintiff)**
	Case	Experian v. I-Centrix
	Project:	Investigating allegations of source code copying and misappropriation of trade secrets.
	Status:	Ongoing
Date:	2005	**Dechert LLP (for Plaintiff)**
	Case	Silvaco vs CSI End Users
	Project:	Analysis and declarations regarding the Defendants' continued use of Silvaco trade secrets.
	Status:	Ongoing
Date:	2005	**DLA Piper (for Defendant)**
	Case	Hynex v. Toshiba
	Project:	Patent infringement investigations (invalidity, claim construction, non-infringement) relating to EDA patent.
	Status:	Ongoing

Patents

Patent Number	Date Issued	Title
6,643,831	2003	Method and system for extraction of parasitic interconnect impedance including inductance
6,381,730	2002	Method and system for extraction of parasitic interconnect impedance including inductance
5,901,063	1999	System and method for extracting parasitic impedance from an integrated circuit layout

Education

Year	College/University	Degree
1987	AEA/Stanford Executive Institute	Completed w/distinction
1979	Stanford University, Stanford, CA	Ph.D., Electrical Engineering
1976	Stanford University, Stanford, CA	MS, Electrical Engineering
1973	Massachusetts Institute of Technology, Boston, MA	BS, Electrical Engineering

Publications

Over fifty articles in the fields circuit design and design automation, including technical papers in peer-reviewed journals, an invited article in the IEEE Spectrum, and various conference proceedings. I have organized seminars, which were designed to enhance the technical credibility of my companies, and written numerous opinion pieces published in journals such as EETimes that served to establish and promote our corporate position.

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Professional Associations and Achievements

- 1999 Fortune Magazine "Cool Company" for Frequency Technology.
- 1984 Electronic Products New Product of the Year award for the Analog Workbench
- 1976 IEEE Microwave Applications award recognizing contributions to the design of GaAsFET amplifiers.

EXHIBIT B

Application-Specific Integrated Circuits

Michael John Sebastian Smith

ADDISON–WESLEY

Boston • San Francisco • New York • Toronto • Montreal
London • Munich • Paris • Madrid
Capetown • Sidney • Tokyo • Singapore • Mexico City

This book is in the Addison-Wesley VLSI Systems Series
Lynn Conway and Charles Seitz, *Consulting Editors*

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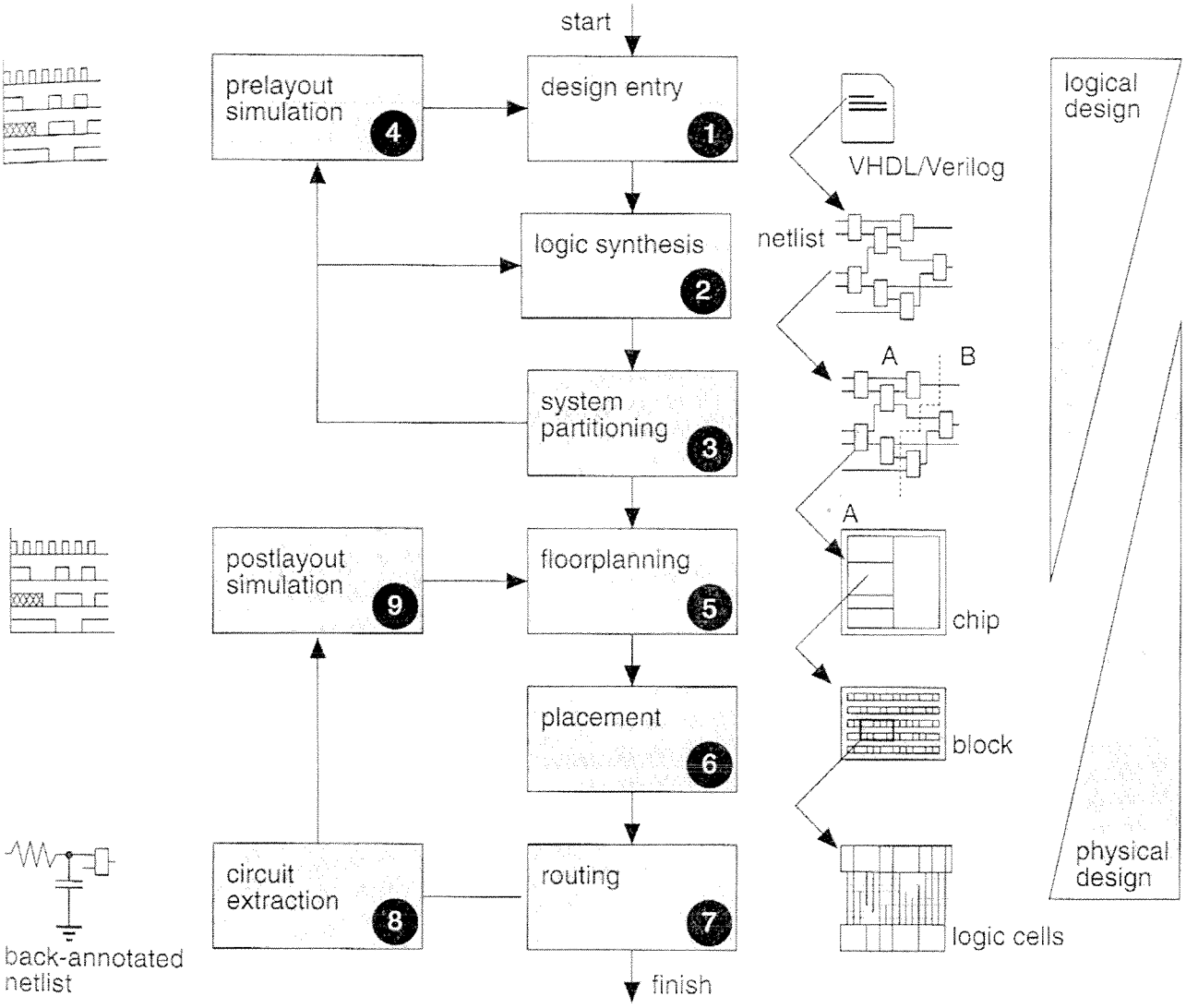

FIGURE 1.10 ASIC design flow.

2. *Logic synthesis*. Use an HDL (VHDL or Verilog) and a logic synthesis tool to produce a **netlist**—a description of the logic cells and their connections.
3. *System partitioning*. Divide a large system into ASIC-sized pieces.
4. *Prelayout simulation*. Check to see if the design functions correctly.
5. *Floorplanning*. Arrange the blocks of the netlist on the chip.
6. *Placement*. Decide the locations of cells in a block.
7. *Routing*. Make the connections between cells and blocks.
8. *Extraction*. Determine the resistance and capacitance of the interconnect.